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****Cache**** control system for ****multi**--**thread**** processor, determines whether ****cache**** is to be shared between processors executing several instruction streams or should be designated for use by single processor
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
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Patent Details:
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Abstract (Basic): JP 2002342163 A
Abstract (Basic):

NOVELTY - The processors execute several instruction streams. A determination unit determines whether a ****cache**** is to be shared between the processors executing several instruction streams or should be designated for use by a single processor.

USE - For controlling access of ****cache**** by ****multi**--**thread**** processors.

ADVANTAGE - ****Reduces**** ****conflict**** between processors in accessing ****cache**** during execution of threads.

DESCRIPTION OF DRAWING(S) - The figure explains assignment of threads for processors. (Drawing includes non-English language text).
pp; 8 DwgNo 2/6

International Patent Class (Main): G06F-012/08
International Patent Class (Additional): G06F-009/46; G06F-012/12
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(11) Publication number:

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PATENT ABSTRACTS OF JAPAN

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(71) Applicant: FUJITSU LTD

(72) Inventor: OGAWARA HIDEKI

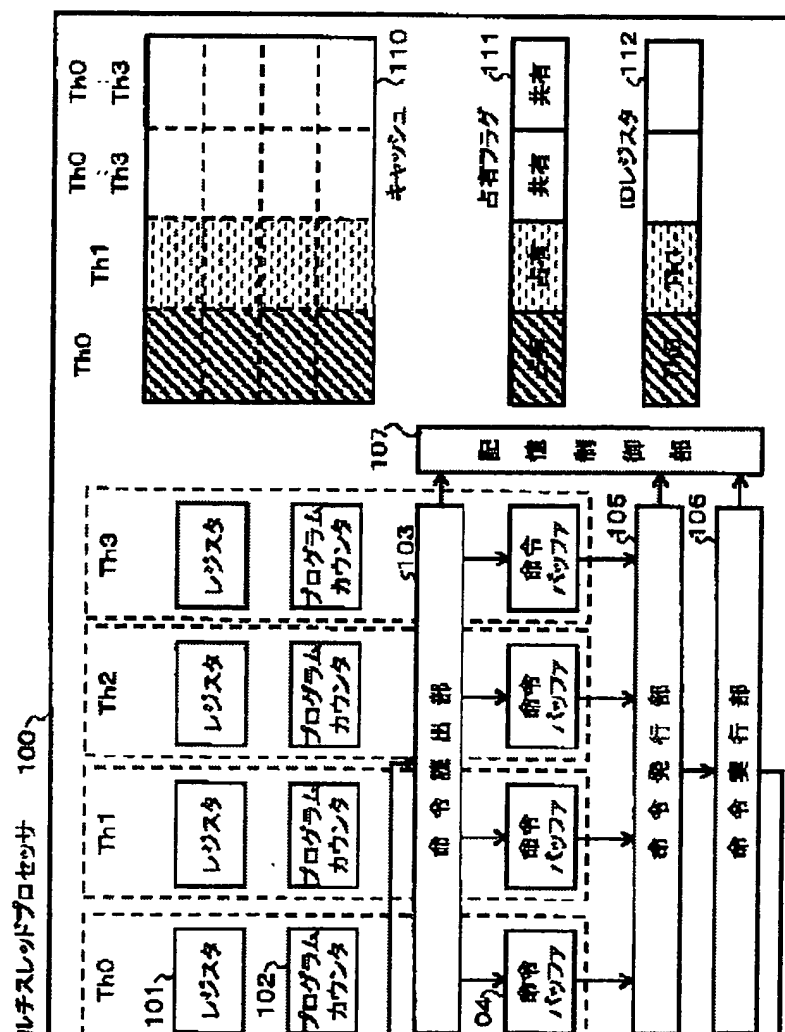
(74) Representative:

(54) METHOD FOR CONTROLLING CACHE FOR MULTITHREAD PROCESSOR

(57) Abstract:

PROBLEM TO BE SOLVED: To realize a control method for effectively utilizing a cache by preventing competition among a plurality of instruction flows about a cache control method for a multithread processor performing the plurality of instruction flows.

SOLUTION: A storage controlling part 107 stores shared/occupied states of threads in an occupancy flag 111 and occupied thread ID in an ID register 112 for each way of a cache 110 according to designation by software, statistical information of



hardware resources, etc. The storage controlling part 107 decides the sharing/occupancy of a corresponding way by using the occupancy flag 111 when a cache error occurs in cache access, and decides whether a self-thread is occupied by using the ID register 112 in the case of occupancy. As a result of the decision, a replacement destination is selected from a way of thread sharing or self-thread occupancy, and data transfer is performed a memory.

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